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(71)(72) Applicant and Inventor: HERBERT, Peter, Anthony, Fry [GB/IE]; Glanville, 21 Summerhill North, Cork (IE).

(74) Agents: O'CONNOR, Donal, H. et al.; Cruickshank & Co., 1 Holles Street, Dublin 2 (IE).

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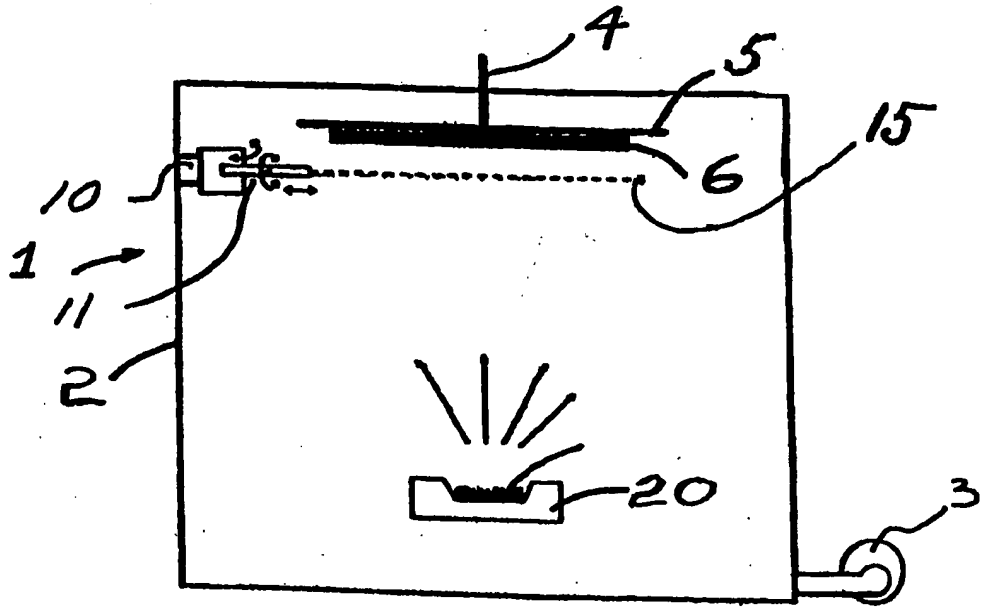

(57) Abstract

A method and apparatus (1) for manufacturing multilayer electrical components (6) such as a multilayer ceramic capacitor. The layers are built up successively in a vacuum chamber (2) by a coating or film deposition process such as the commonly used thin film coating technology by using a spatially movable mechanical shadow mask (15). This enables the pattern to be changed from layer to layer without breaking the vacuum.

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"A Method and Apparatus for the Production of Multilayer Electrical Components"

Introduction

The present invention relates to a method and apparatus for the production of multilayer electrical, electronic or optical components hereinafter electrical components, usually formed in layers of alternate materials or combinations of materials on a substrate layer. The method used comprises applying the layers of material in a vacuum by a deposition or coating process, usually with one layer substantially covering the previous layer and the next layer being formed with a substantially sheet-like apertured mask interposed between the previous layer and a material source for application of the next material followed by subsequent fabrication into the desired component.

For example, in the electronics component industry, there are a wide variety of production techniques for components of the type having interleaved conductive and dielectric elements. It is known to produce a multilayer ceramic capacitor (MCC) by screen printing a conductive ink onto one side of a dielectric tape to form a conducting overlay and hence an electrode leaf. The printed tape with this electrode leaf is then cut into sheets and selectively stacked before being compressed between platens and diced into individual chips along cut lines. The chips are then fired to drive away the volatile components and sinter the dielectric ceramic. Interconnection of the conductive elements of the chips is then provided before packaging of the component is completed.

While this process does produce a component with interleaved conductive and dielectric elements it presents manufacturers with a number of problems. The principal problem is the cost associated with producing such components which is high because of the number of steps involved and the difficulties in handling the materials. These costs are further increased due to the relatively poor yield of such processes and the complexity of dealing with the chemicals involved. Additionally, the thick film nature of existing processes means that the choice of fabrication materials is limited.

With the ongoing trend in electronic device development towards miniaturisation, current production processes suffer a particular problem in that there is an ongoing need to optimise the use of available circuit board real estate. Developing suitably small components is difficult with current techniques. This is particularly the case when a high performance characteristic is required, for example, the physical limitations when making capacitors. The quantity of charge which can be stored on a capacitor is limited by the area of conductive plates, the dielectric constant of the material between the plates, the inter-plate spacing and the dielectric strength of the material used. While these limitations may be readily overcome where cost is not an issue and where sufficient space on a printed circuit board is available, however, where this is not the case current techniques are not appropriate.

In the manufacture of capacitors, a thin film process for putting down both dielectric and metal layers would be highly advantageous as it would enable an increase in capacitance and a decrease in capacitor size. Many thin film coating techniques are available which cannot be used in this application to manufacture, for example, multilayer capacitors, because of the need to individually pattern each single layer of the multilayer stack. This has heretofore been done ex-situ doing each layer one at a time.

The present invention is directed towards providing a process and apparatus using conventional vacuum based film deposition or coating techniques to manufacture multilayer electrical components such as capacitors.

Statements of Invention

According to the invention, there is provided a method for the production of multilayer electrical components usually formed in layers of alternate materials or combinations of materials on a substrate layer comprising applying the layers of material in a vacuum chamber by a deposition or coating process usually with one layer substantially covering the previous layer and the next layer being formed with a substantially sheet-like apertured mask interposed between the previous layer and a material source for application of the next material followed by subsequent fabrication

into the desired component characterised in that the steps are performed of:-

moving the mask to a mask present position between a layer and the material source to interpose the mask between the material source and the layer;

applying the material to form the next layer;

moving the mask to a mask remote position relative to the now uppermost layer to allow formation of the next layer; and

maintaining the vacuum in the chamber.

The advantage of this in situ patterning during the coating/film deposition process by a spatially movable, mechanically fabricated shadow mask placed over the substrate on which the multilayer structure is being deposited, enables the area geometry or coverage of each individual film or layer to be controlled in turn without having to break the vacuum or remove the workpiece to carry out an alternative patterning process in each layer prior to deposition of the next layer.

According to the invention, there is provided a method in which the mask is alternatively moved from the mask present position to the mask remote position. This is a particularly suitable process for manufacturing a multilayer capacitor. It will be appreciated that polymer and ferro electric ceramic dielectrics can be easily applied by this process and will offer more compact designs than can be produced with more conventional dielectric material.

Ideally, in the method according to the invention, the mask is moved to assume different positions relative to the material source in the mask present position to define at least two different patterns of material layer with the mask present. In this latter method, for example, where one is producing a multilayer ceramic capacitor which is simply a monolithic block of ceramic containing two sets of offset interleaved planar electrodes that extend for two opposite surfaces of the ceramic dielectric parallelepiped so formed, a simple back and forth movement using a mask having a plurality of longitudinally arranged slits will be sufficient to provide the two end portions

to form the interleaving.

Ideally, the mask is moved laterally and substantially parallel to the uppermost layer. This is particularly suitable for the making of multilayer ceramic capacitors.

In another method according to the invention, the mask is pivoted relative to the upper layer. In this way, various different shapes can be made. Indeed, by moving the mask, all sorts of shapes can be provided and thus, for example, where the alternate layers do not have the identical pattern, it would be possible to provide different patterns on different layers which might be required for certain components.

According to the invention, it is envisaged that prior to applying a layer of material in the mask present position, the additional step is performed of choosing a mask from at least two masks stored in the vacuum chamber. Obviously, if different masks can be chosen, even more versatility can be provided.

Ideally, when the mask is not required for the next mask present application of a layer of material, the mask is stored in a remote position in the vacuum chamber.

Preferably, in the application of material to form a layer in the mask present position, the method comprises the additional steps of:-

stopping the application of material by the material source;

moving the mask relative to the material source; and

recommencing the application of material.

In this way, various different thicknesses of material can be applied on the one layer. Ideally, the application of at least one layer involves the application of at least two separate materials from separate material sources. Again, considerable versatility can be provided.

Further, the invention provides apparatus for the manufacture of a multilayer electrical

component by deposition or coating of the type comprising:-

a chamber;

means for maintaining the chamber under a vacuum;

a workpiece carrier;

a material applicator mounted in the chamber; and

a mask holder assembly having an apertured mask as part thereof:

characterised in that there is provided means for moving the mask holder assembly from a mask present position with the apertured mask interposed between the workpiece and the material applicator to a mask remote position.

By maintaining the vacuum in the chamber all the time, the whole process can be mechanised and automated and thus greatly increase the production throughput.

Preferably, means are provided for moving the mask holder assembly in the mask present position to vary the pattern of material applied to the workpiece. By allowing the mask not just simply to be placed in one position all the time, it is possible to vary the pattern.

In a still further embodiment of the invention, the mask holder assembly carries at least two separate masks and includes means for selectively choosing the appropriate mask for application of material. Again, this adds further versatility.

Further, the invention provides an apparatus in which a mask comprises at least two separate patterns of apertures to form layers of different pattern.

Detailed Description of the Invention

The invention will be more clearly understood from the following description of some embodiments thereof given by way of example only with reference to the accompanying drawings in which:

Fig. 1 is a diagrammatic view of an apparatus for use in the invention;

Fig. 2 is a plan view of a shadow mask used in the apparatus of Fig. 1;

Figs. 3(a) to (g) are diagrammatic views of a workpiece detailing the various stages of the manufacture of a multilayer capacitor in accordance with the invention;

Fig. 4 is a flow diagram illustrating some steps in the fabrication of the multilayer capacitor in accordance with the invention;

Fig. 5 is a diagrammatic view of an alternative construction of apparatus according to the present invention; and

Fig. 6 is a plan view of an alternative construction of mask according to the invention.

For the purpose of this specification the process of the invention is described with particular reference to the production of a multilayer capacitor. It will be readily apparent to those skilled in the art that the process may equally be applied to the production of many other components where inter-leaving is required, for example in the production of transformers, inductors or other microelectronic circuits or electronic components or optical devices.

Referring to Figs. 1 to 4 inclusive and initially to Fig. 1, there is provided an apparatus 1 which comprises a vacuum deposition chamber 2 having an evacuation pump 3 and a workpiece carrier 4 incorporating a platen 5. A workpiece 6 is illustrated mounted on the platen 5. A mask holder assembly 10 is mounted within the chamber 2 and

mounts a mask support 11 which in turn carries an apertured planar mask 15. The mask holder assembly 10 and mask support 11 are of essentially conventional construction and can be of any suitable mechanical construction and ideally include means for moving the mask support 11 in and about any axis. A material applicator 20, in this embodiment, a plasma enhanced chemical vapour deposition device, is mounted in the vacuum deposition chamber 2 remote from the workpiece carrier 4. All of the components are of conventional construction and do not require any further description.

Referring now to Fig. 2, the mask 15 incorporates a plurality of longitudinal apertures 16 and again is of conventional construction.

Referring now to Figs. 3 and 4, the method according to the present invention for the production of multilayer electrical components is described with reference to a process for manufacturing a multilayer capacitor. Not all of the production of the capacitor is described but simply the deposition of the conductor and dielectric layers so as to produce a composite sheet which then has to be cut up to produce individual units, often referred to as dices, which in turn have their electrode leaves interconnected by metalisation, connectors attached and then encapsulated in some way in plastics to produce a multilayer capacitor.

Referring now to Fig. 1 specifically, the workpiece 6 is loaded onto the platen 5 of the workpiece carrier 4 in step 100. The chamber 2 is then evacuated in step 101 by the evacuation pump 3. The mask holder assembly 10 is operated in step 102 to move the shadow mask to an un-masked mode, namely, to a mask remote position relative to the workpiece. This is illustrated in Fig. 3(a) where dielectric is deposited, deposition being illustrated by arrows in Fig. 3 and by step 103 in Fig. 4. In step 104, the deposition of the dielectric is terminated and the dielectric layer 25 is now fully formed. The mask holder assembly 10 is then activated in step 105 to place the mask 15 in the correct position as shown in Fig. 3(b). In step 106, the material applicator 20 is activated to deposit a conductive layer indicated by the reference numeral 26 and in step 107 the deposition of the conductive layer is terminated and the conductive layer 26 is now ready to receive, if required, another layer of dielectric.

The various steps 102 to 107 are then repeated until sufficient layers of dielectric 25 and conductive material 26 are added so that if the steps are carried out, for example, ten times, they will produce two interleaved five leaf electrode structure. Finally, the last layer deposited must be a dielectric layer. It will be appreciated that this is achieved in the present apparatus by successfully toggling the mask 15 by the mask holder assembly 10 into a mask present and a mask remote mode of operation. It will be noted that in the manufacture of the capacitor according to the present invention that the use of the mask 15 has to be so arranged to ensure that there is adequate interconnection between the conductive layers forming one of the multi-leaf electrodes, but no interconnection between leaves belonging to different electrodes.

Thus, for example, referring again to Fig. 3 (d), there is illustrated a conductive layer 26 on top of a dielectric layer 25 and a further dielectric layer 25 between the first conductive layer 26 and the second conductive layer 26. It will be noted that the mask 15 is laterally displaced to the left in Fig. 3(d) relative to the position taken in Fig. 3(b). Fig. 3(e) shows the deposition of a further dielectric layer 25 while Fig. 3(f) shows the deposition of a still further conductive layer 26. Fig. 3(g) illustrates the deposition of dielectric material 25. When sufficient conductive and dielectric material 25 have been deposited, the resultant workpiece may be cut into dices which are then used to form a capacitor.

Referring now to Fig. 5, there is illustrated an alternative construction of apparatus indicated generally by the reference numeral 30 in which parts similar to those described with reference to the previous drawings are identified by the same reference numerals. In this embodiment of the invention, there is provided a mask storage area 31 housing two additional masks 6(a) and 6(b). In this embodiment, the mask holder assembly 10 chooses the particular mask required. It is envisaged that in certain situations, different constructions of masks may be required to provide the necessary pattern.

Referring now to Fig. 6, there is illustrated an alternative construction of apertured planar mask indicated generally by the reference numeral 40, which planar mask is effectively divided into two separate sections having apertures 41 and 42 of different sizes. Thus, two different patterns can be provided by the same mask. It will be

appreciated, for example, with the mask as illustrated in Fig. 2, that tilting the mask relative to the workpiece would have the same effect on the pattern as providing narrower apertures.

It will be appreciated that the real advantage of the present invention is the application simply of vacuum based film deposition or coating techniques to the manufacture of such components. In situ patterning during the coating or film deposition process by a spatially movable mechanical shadow mask placed over the substrate upon which the multilayer structure is being deposited enables the area geometry or coverage of each individual film or layer to be controlled in turn without having to break the vacuum or remove the workpiece to carry out an alternative patterning process on each layer prior to deposition of the next layer. It enables technically powerful thin film coating technology to be applied to the manufacture of multilayer capacitors involving the usage of advanced materials not currently possible.

While considerable emphasis has been placed on the manufacture of capacitors, it must be appreciated that the invention is not limited to capacitors as has been mentioned throughout the specification. The reason why capacitors have been chosen for illustrative purposes is that they are one of the most commonly used devices and in particular the general trends of geometry and material selection are such as to make the manufacture of multilayer capacitors having a thin dielectric layer of high dielectric constant or strength particularly advantageous with the present invention. Thus, the present invention allows the use of new high dielectric constant or strength materials in thin layers which allows the increase of capacitance without corresponding component increases in thickness.

It will be appreciated that the manufacturing process according to the present invention is a relatively simple process using of the order of six main steps which in turn reduces costs. Further, since thin film coating technology is already well developed, any process that utilises a well known technology is of its nature going to lead to high manufacturing yield.

The present invention obviates the need to use weak ceramic solvents and organic binders and the need for high temperature firing. Further, the elimination of high

temperature sintering reduces the cost of materials. Further, in accordance with the present invention, a much wider range of materials can be used allowing for increases in the efficiency of many devices. As has been mentioned above, this increase in efficiency and performance is particularly applicable to capacitors.

The present invention allows the manufacture of devices for many new applications including ignition systems, lasers, X-ray generation, power supplies, and indeed many other pieces of equipment.

Various constructions of vacuum deposition chambers may be used such as are commercially available, for example, from Balzers of Liechtenstein, Temescal of USA and Leybold Heraeus of Germany. Similarly, many deposition sources may be used and indeed multiple deposition sources may be used which could include, for example, electron-beam thermal evaporation, Knudsen cell, resistance heater thermal evaporation, sputtering, Chemical Vapour Deposition, Plasma enhanced Chemical Vapour Deposition and Ion Gun techniques such as Ion Beam Sputtering and Ion Assisted Deposition. Multiple deposition sources in the vacuum chamber may also be used. For example, in the fabrication of a capacitor one source may be used for the dielectric and another source for the conductor. Similarly, it is possible to use co-deposition from two courses to obtain a particular film composition or stoichiometry. Generally speaking, the shadow masks are of a regular solid planar material but indeed any suitable shadow mask could be used. While in the embodiment described above, there has been no particular description of the mask holder assembly, it will be appreciated that the mask holder assembly would be controlled by conventional control methods such as computer control devices and by any form of coupling linking. Many different forms of mechanical actuators such as push-pull rods, rotating pivots and/or x-y-z-θ stepper motors could be used. Again, many forms of locating devices can be used in the vacuum chamber to ensure that the mask is correctly located relative to the workpiece. It will also be appreciated that the shadow mask may be designed in any particular way to provide the necessary deposition pattern. It will also be appreciated that the shadow mask can be moved so that coating is prevented or interrupted over any chosen sequence of selected areas of a workpiece. This enables the patterning of the coating film or films being deposited by material from the material source onto the workpiece in situ within the chamber during the

process.

It is an important feature of the invention that the workpiece can thus be selectively coated with suitable material within the chamber to a desired pattern in real time in-situ within the chamber during the coating process. A further important feature is the way in which the mask may be moved both between masked and un-masked modes of operation and between a variety of different masking positions to achieve the desired pattern and that if desired different materials from the material applicator or material source may be used to coat or etch the workpiece in accordance with the position of the mask. It will be appreciated that in addition to the deposition or coating described that selective use of an etch material or etching techniques such as sputter etching may also be used to achieve the required patternation.

The present invention allows for the use of materials heretofore deemed not suitable for the manufacture of such devices. In addition to reducing costs, it allows for the use of materials whose performance characteristics enhance the operation of the final device. For example, given the limiting factors on capacitor performance imposed by the dielectric constant or strength of the material used the invention allows for the use of materials with very high dielectric constant or strength allowing an increase in device capacitance and hence in energy storage capacity. Furthermore there is a reduction in device size and an improvement in performance. The invention allows for significantly increased manufacturing parameter space which allows the device parameters relating to dielectric constant, inter-plate spacing and dielectric strength to be varied over far wider ranges than currently. This allows enhanced device customisation for applications, including ignition systems, lasers, x-ray generation, scientific research, power suppliers, electric vehicles, solar-powered equipment and medical applications e.g. cardiac defibrillation.

Thus, for example, the use of new, high dielectric strength material allows high capacitance to be obtained by reduction of inter plate spacing while maintaining acceptable breakdown voltage, Vm. Fast capacitor discharge is also possible because of the small inter-plate spacing and use of the high purity dielectric materials now possible with the invention will give low leakage currents. Improvement in manufacturing tolerances is obtained by using for process control thin film deposition

parameters such as physical or optical thicknesses which can be accurately monitored during deposition by a variety of techniques, such as quartz crystal monitoring, to very high accuracy. Additionally the production of ultra-high purity, high quality dielectric films which are free from pinholes and other intrinsic defects is standard in the thin film coating industries such as microelectronics and optical coating. The process is, thus, inherently high yield and obviates the requirement for complete component testing as is currently standard. For many requirements such as PCB manufacture and memory backups a high capacitance per unit volume is required. The process is thus particularly suited to this type of application and as the devices produced in accordance with the invention are solid-state devices with excellent thermal and mechanical properties they are thus good for harsh environments. The lifetimes in terms of charge-discharge cycles of capacitors produced in accordance with the invention is orders of magnitude longer than those of current multilayer capacitors.

To produce many interleaved electrode structures, the shadow mask is replicated as desired in the x-y plane (e.g. laterally across a planar workpiece) to cover the entire area of the workpiece with suitable spacing between masking elements according to designed capacitor schematic. The workpiece is then cut to leave suitably exposed conductive elements for each of the capacitors produced which are then metal interconnected, bonded and finished using conventional techniques.

For illustrative purposes one embodiment of invention comprises an electron-beam evaporation with two materials Titanium Dioxide (TiO_2) and Aluminium. The chamber 2 can be filled with a partial pressure of Oxygen during the dielectric evaporation to maintain the stoichiometry of the TiO_2 during evaporation. Deposition is carried out by alternate evaporation of the materials using the electron beam and the thickness of the evaporation is monitored using a quartz crystal monitor. Five hundred layers of 1 micrometre thick TiO_2 are deposited with interleaved Aluminium layers of 0.5 micrometre thick in the process of the invention. These layers are deposited on a suitable substrate, such as for example Silicon, with a substrate thickness of 350 micrometres.

The substrate can be patterned, by means of the shadow mask, to produce capacitors

of the required dimension. This would allow a maximum operational rating of 10 Volts. In this way, from a 1 m^2 area of substrate, 10,000 capacitors of 76 µF can be produced with dimensions of 1 cm x 1 cm x 1.1 mm. Alternatively, 1,000,000 capacitors of dimension 1 mm x 1 mm x 1.1 mm can be fabricated with a capacitance 0.76 µF.

These capacitors can be stacked to give a capacitance of 690 µF per cm^3 which is competitive in volume terms with electrolytic capacitors and at a lower cost.

The voltage rating of the capacitors can be improved by producing thicker dielectric layers albeit with a corresponding decrease in the capacitance values. For example one hundred layers of 5 µm thick TiO_2 will give a maximum voltage rating of 50 Volts with a capacitance of 3.04 µF per cm^2 of fully coated substrate or 33 µF per cm^3 for stacked devices. In other embodiments high dielectric constant, high dielectric strength dielectrics can be used such as Barium or Strontium Titanate. Deposition of these materials can be carried out by stoichiometric co-evaporation of Barium/Strontium and TiO_2 followed by a post-sintering of the stack to form crystalline dielectric material. In this case the interleaved metal would need to be a high melting point metal such as Palladium or Platinum. Specially formulated ceramics such as Z5U, plasma polymerised hexamethyldisilazane (pp HMDSN) and hexamethyldisiloxane may also be used. For illustration, 500 layers of 1 micrometre thick ppHMDSN deposited with interleaved Aluminium layers of 0.5 micrometre thick on a 350 micrometre thick Silicon substrate will give a capacitance per cm^2 of 2.04 microFarads with a breakdown voltage Vm of approximately 60kV. These capacitors have an energy storage capacity of 25 MJ/m^3 and can be stacked to give an capacitance of 18.5 microFarad per cm^3.

It will be apparent that the process of the invention may be varied by altering the shadow mask design, layout and patterning. It will further be appreciated that a sequence of different film depositions, including but not limited to codeposition and deposition of multiple (more than two) materials may be used. The relative timing of shadow mask positioning versus individual film deposition to produce film composition varying spatially in all geometrical co-ordinate directions, e.g. (x, y, z) or (θ, z), etc. producing for example, laterally (x-y plane) or vertically (z direction) graded structures may also be varied. The moveable, in-situ-coating shadow mask patterning process

enables capacitor mass manufacturing to access the technical and commercial advantages of the powerful thin film coating technology sector.

The process of the invention is significantly simplified to reduce cost. Due to the well-developed, mature and robust nature of thin film coating technology, manufacturing yield is high reducing costs and testing requirements.

Advantageously the use of weak ceramic tape, solvents and organic binders and the need for high temperature firing is eliminated. Furthermore the elimination of high temperature sintering allows the use of low cost metals and the use of a thin film process (layers down to nanometre thickness are possible) allows the design of high capacitance, high energy storage capacity devices by reduction of dielectric thickness parameter, an improvement in performance and a reduction in size and cost.

The terms "include, including, includes and included" and the terms "comprise, comprising, comprises and comprised" are used interchangeably in this specification and should be afforded the widest possible interpretation.

The invention is not limited to the embodiments or methods hereinbefore described but may be varied in construction and detail within the scope of the claims.

CLAIMS

1. A method for the production of multilayer electrical components usually formed in layers of alternate materials or combinations of materials on a substrate layer comprising applying the layers of material in a vacuum chamber by a deposition or coating process usually with one layer substantially covering the previous layer and the next layer being formed with a substantially sheet-like apertured mask interposed between the previous layer and a material source for application of the next material followed by subsequent fabrication into the desired component characterised in that the steps are performed of:-

   moving the mask to a mask present position between a layer and the material source to interpose the mask between the material source and the layer;

   applying the material to form the next layer;

   moving the mask to a mask remote position relative to the now uppermost layer to allow formation of the next layer; and

   maintaining the vacuum in the chamber.

2. A method as claimed in claim 1, in which the mask is alternatively moved from the mask present position to the mask remote position.

3. A method as claimed in claim1 or 2, in which the mask is moved to assume different positions relative to the material source in the mask present position to define at least two different patterns of material layer with the mask present.

4. A method as claimed in claim 3, in which the mask is moved laterally and substantially parallel to the uppermost layer.

5. A method as claimed in claim 3 or 4, in which the mask is pivoted relative to the upper layer.

6. A method as claimed in any preceding claim, in which prior to applying a layer of material in the mask present position, the additional step is performed of choosing a mask from at least two masks stored in the vacuum chamber.

7. A method as claimed in claim6, in which when the mask is not required for the next mask present application of a layer of material, the mask is stored in a remote position in the vacuum chamber.

8. A method as claimed in any preceding claim, in which on the application of material to form a layer in the mask present position, the method comprises the additional steps of:-

stopping the application of material by the material source;

moving the mask relative to the material source; and

recommencing the application of material.

9. A method as claimed in any preceding claim, in which the application of at least one layer involves the application of at least two separate materials from separate material sources.

10. Apparatus for the manufacture of a multilayer electrical component by deposition or coating of the type comprising:-

a chamber;

means for maintaining the chamber under a vacuum;

a workpiece carrier;

a material applicator mounted in the chamber; and

a mask holder assembly having an apertured mask as part thereof:

characterised in that there is provided means for moving the mask holder assembly from a mask present position with the apertured mask interposed between the workpiece and the material applicator to a mask remote position.

11. Apparatus as claimed in claim 10 in which means are provided for moving the mask holder assembly in the mask present position to vary the pattern of material applied to the workpiece.

12. Apparatus as claimed in claim 10 or 11, in which the mask holder assembly carries at least two separate masks and includes means for selectively choosing the appropriate mask for application of material.

13. Apparatus as claimed in any of claims 10 to 12, in which a mask comprises at least two separate patterns of apertures to form layers of different pattern.

14. An electrical component manufactured in accordance with the method as claimed in any of claims 1 to 9.

15. An electrical component manufactured with the apparatus as claimed in any of claims 10 to 13.

16. An electrical component as claimed in claim 14 or 15 in which the component is a multilayer capacitor.

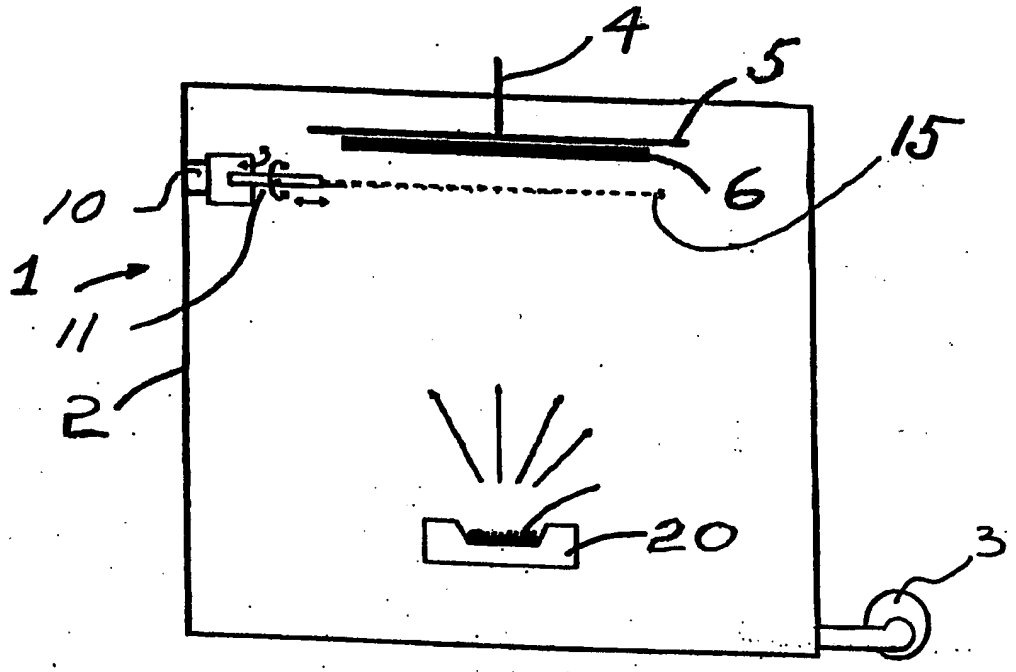


Fig. 1

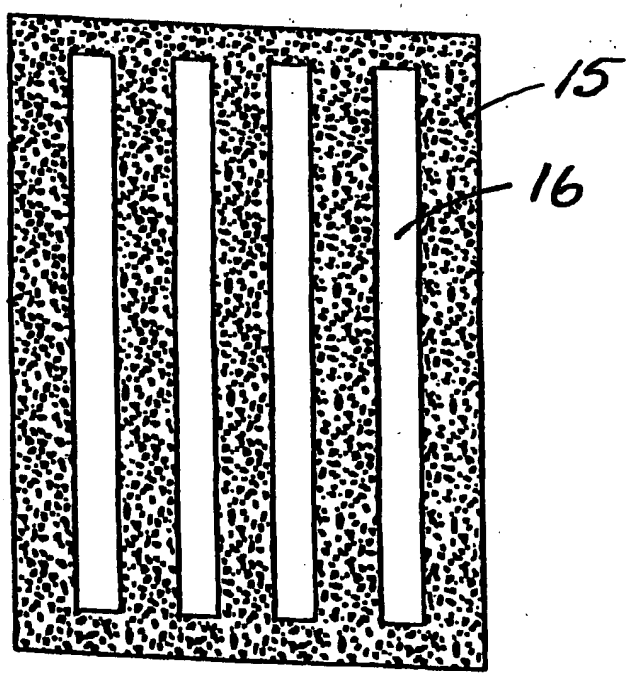


Fig. 2

Fig. 3(a)

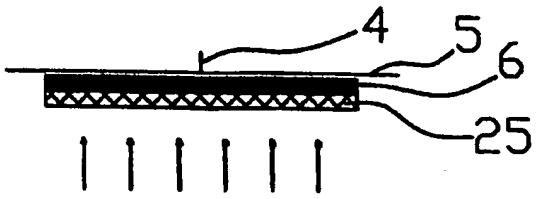


Fig. 3(b)

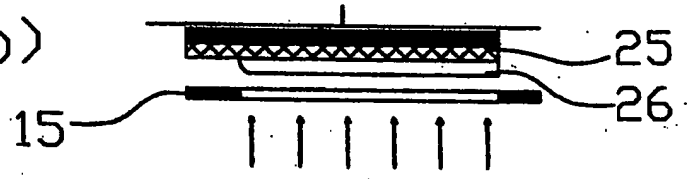


Fig. 3(c)

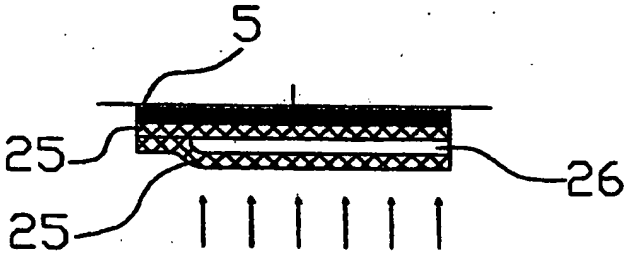
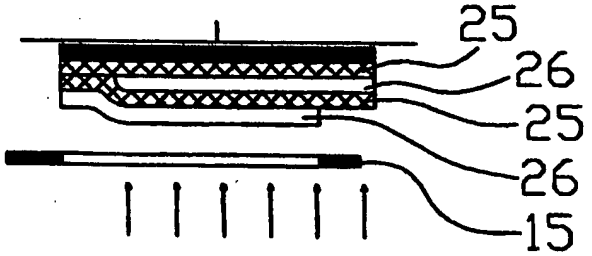


Fig. 3(d)



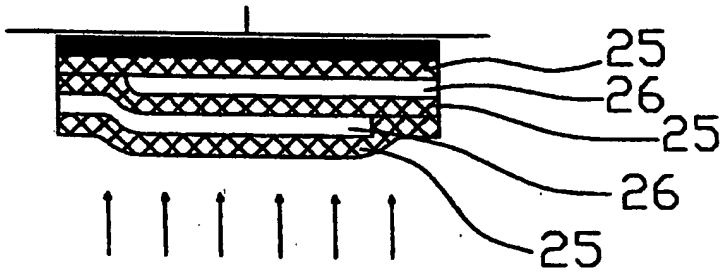


Fig. 3(e)

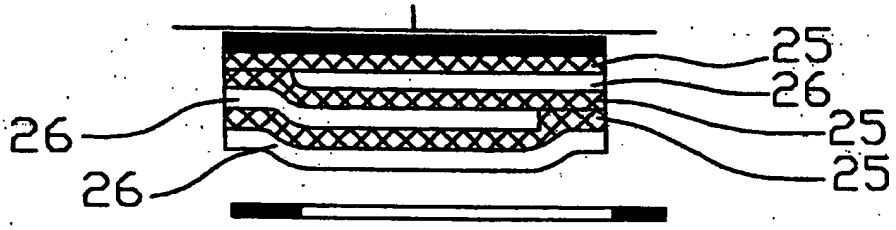


Fig. 3(f)

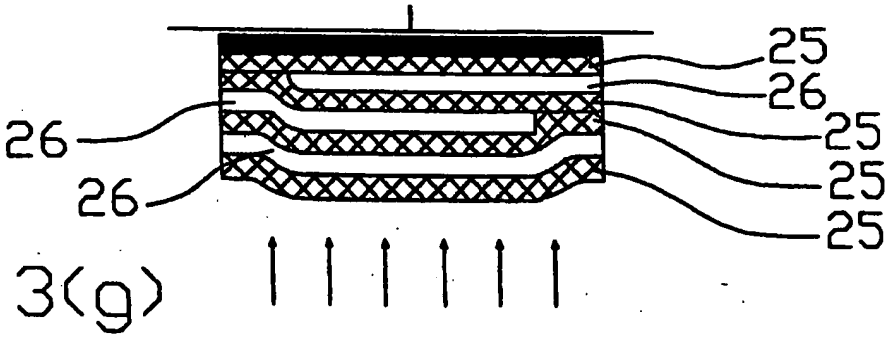


Fig. 3(g)

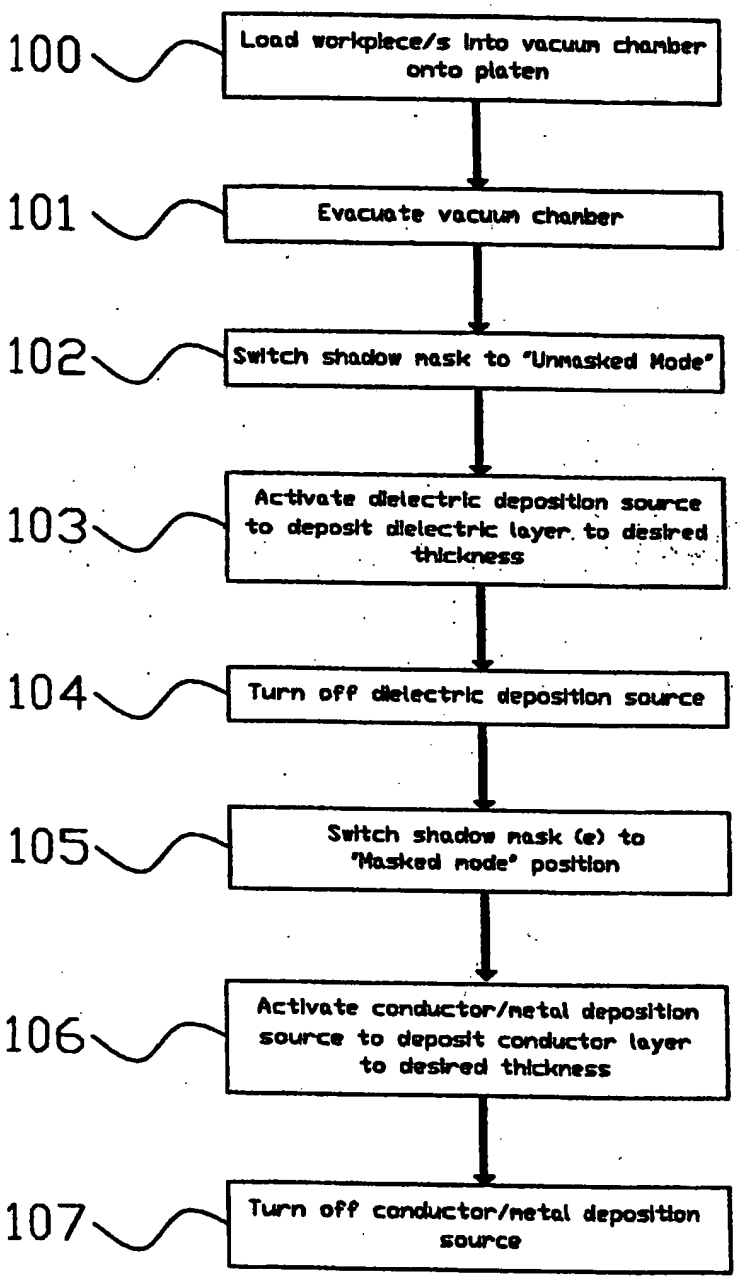

100
Load workpiece/s into vacuum chamber onto platen
101
Evacuate vacuum chamber
102
Switch shadow mask to "Unmasked Mode"
103
Activate dielectric deposition source to deposit dielectric layer to desired thickness
104
Turn off dielectric deposition source
105
Switch shadow mask (e) to "Masked mode" position
106
Activate conductor/metal deposition source to deposit conductor layer to desired thickness
107
Turn off conductor/metal deposition source

Fig. 4

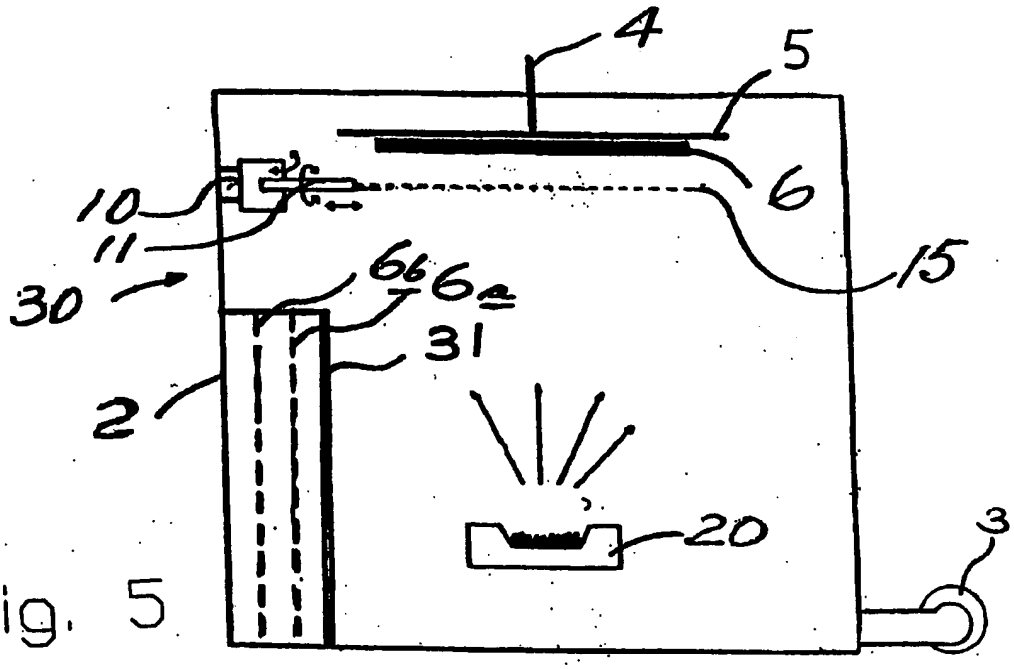


Fig. 5

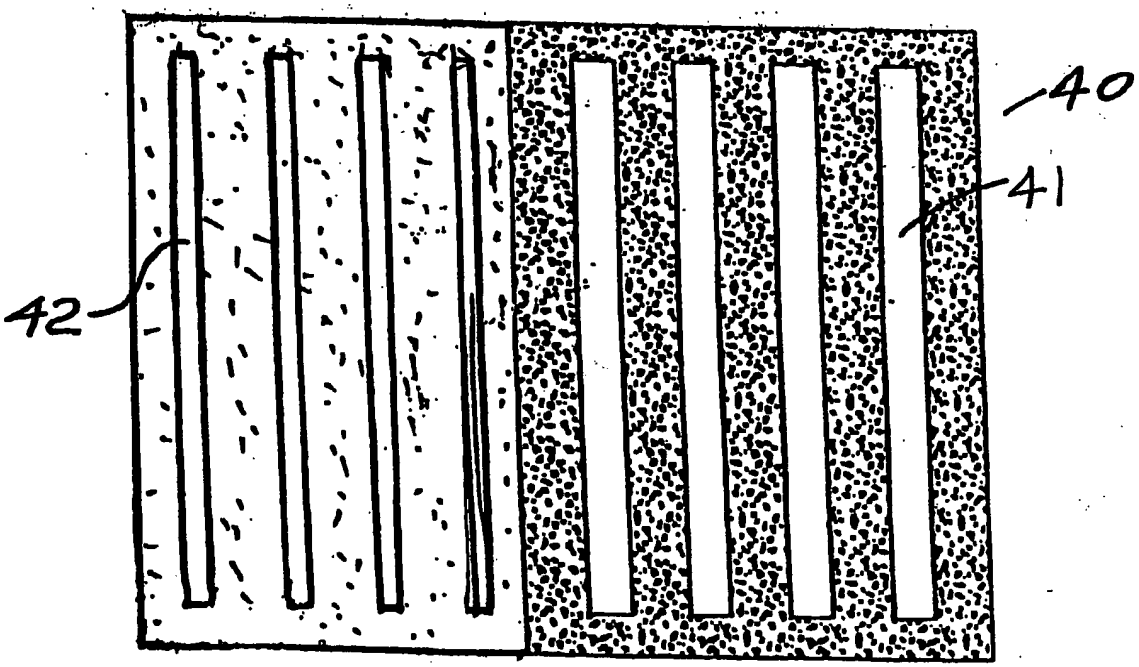


Fig. 6

INTERNATIONAL SEARCH REPORT

Int tional Application No
PCT/IE 98/00102

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01G4/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01G C23C H01L H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 147 696 A (GEN ELECTRIC) 10 July 1985 see page 6, line 27 - line 34 see page 8, line 21 - page 9, line 27 see figures 2-4,13	1-5, 8-11, 13-16
Y	---	6,7,12
Y	DE 29 03 292 A (SIEMENS AG) 7 August 1980 see page 3, line 14 - page 4, line 5 see page 4, line 30 - page 5, line 6 see page 6, line 7 - line 18 see figure 1	6,7,12

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 March 1999	12/03/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Goossens, A

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ional Application No
PCT/IE 98/00102

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